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High-aspect ratio through-silicon vias for the integration of microfluidic cooling with 3D microsystems

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ABSTRACT

Microfluidic cooling technology is a promising thermal solution for high-performance three-dimensional integrated circuits (3D ICs). However, the integration of microfluidic cooling into 3D ICs inevitably impacts tier-to-tier through-silicon vias (TSVs) by increasing their length and diameter (for a fixed aspect ratio). To address this challenge, this paper presents the fabrication of very high-aspect ratio (23:1) TSVs within a microfluidic pin-fin heat sink using two types of silicon etch masks. Void-free TSVs are electrically characterized using X-ray inspection and four-point resistance measurements.

1. Introduction

Three-dimensional integrated circuit (3D IC) technology has recently attracted considerable interest as a "More-than-Moore" solution [1,2]. The through silicon via (TSV) is a key component of 3D ICs; it offers decreased latency, decreased energy-per-bit, and increased bandwidth density [3–5]. However, one of the existing limitations to the realization of high-performance 3D ICs is the difficulty to dissipate generated heat since 3D ICs have limited thermal paths to the ambient compared to two-dimensional (2D) ICs. To this end, interlayer microfluidic cooling is widely explored as a means to address these thermal constraints. Microfluidic cooling was first shown by Tuckerman and Pease in 1981 [6], and since then, additional studies have presented the feasibility of microfluidic cooling for removing heat in single- and multiple-tiered chips [7–10].

When it comes to the integration of microfluidic cooling within 3D ICs, TSV aspect ratio is a key parameter that determines TSV electrical parasitics. Typically, to achieve higher cooling capability, a microfluidic heat sink requires each chip to be relatively thick, since the height of the heat sink is strongly related to its cooling capability. In prior work, the thickness of dice with an embedded microfluidic heat sink was shown to be a few hundred micrometers [6–11]. While such thickness is attractive from a thermal point of view, this inevitably increases TSV dimensions (diameter and height) and thus, TSV capacitance, which impacts latency and energy dissipation. Moreover, as a TSV diameter increases, the number of TSVs that can be placed in a heat sink, or a bandwidth density of I/Os, quadratically decreases between stacked ICs. Thus, small TSV dimensions are preferable since they not only minimize the silicon real-estate footprint, but they also improve the electrical performances. While prior work has shown the integration of TSVs in a microfluidic heat sink [9,11], the reported TSVs were very large in diameter (50–60 μm) and with an aspect ratio of only 5:1, leading to large electrical parasitics. Prior work [10] shows preliminary effort in the fabrication of 18:1 aspect ratio TSVs within a microfluidic heat sink. However, these TSVs were not electrically isolated and were not completely etched through the wafer due to innate difficulty in high-aspect ratio silicon etching and copper filling for a thick silicon substrate. Prior work [12] shows preliminary efforts on the integration of microfluidic cooling with 3D ICs. In addition, different approaches to the formation of high-aspect ratio (HAR) TSV fabrication have been proposed including nickel wires or wire bonds [13,14]. However, these TSV techniques require additional fabrication steps for BCB polymer formation between the TSV cores and the silicon.

This paper focuses on the fabrication of the fully isolated TSVs with an aspect ratio of 23:1 and investigates the integration of the HAR TSVs within a microfluidic heat sink using various fabrication processes. In Section 2, we propose a 3D system with TSVs embedded within interlayer-microfluidic cooling. Section 3 describes the fabrication in detail and electrical characterization of HAR TSVs within a micropin-fin heat sink; this is done using two different masking methods during the silicon etching step. Void-free TSVs are validated using four-point

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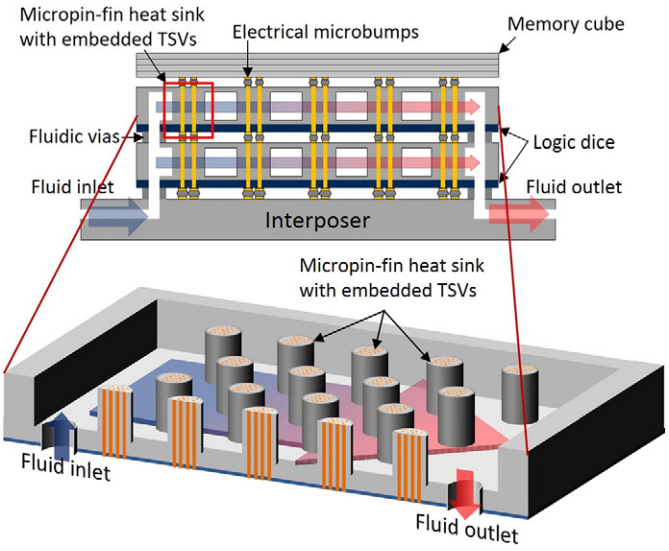

Fig. 1. A schematic of the proposed 3D system with embedded microfluidic cooling.

resistance measurements and X-ray imaging, and conclusions are presented in Section 4.

2. A proposed 3D microsystem: Need for high-aspect ratio TSVs

Fig. 1 illustrates a potential 3D electronic microsystem in which two logic dice and a memory cube are stacked on an interposer substrate. Each logic die consists of a micropin-fin heat sink with integrated TSVs for electrical connectivity. Fluidic vias are also formed in the dice

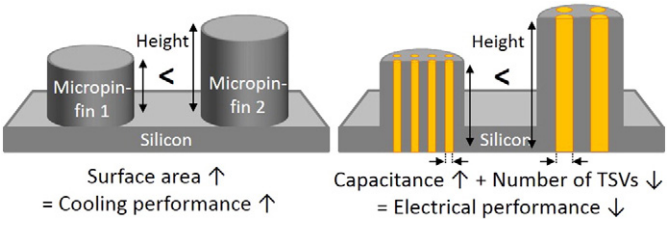

Fig. 2. Trade-off exists between electrical and thermal performances with respect to the height of silicon micropin-fins.

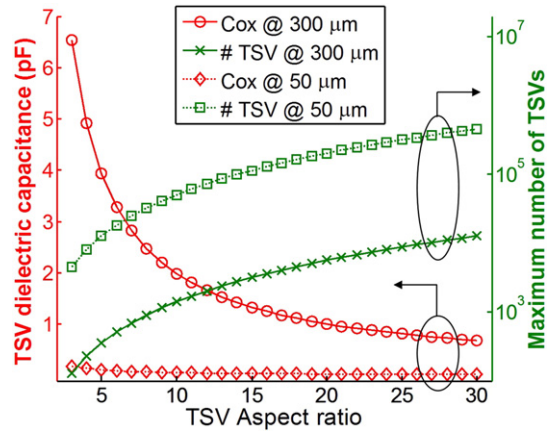

Fig. 3. TSV dielectric capacitance and maximum number of TSVs as a function of aspect ratio and die thickness (TSV diameter and oxide thickness are 13 and 0.5 μm, respectively).

Table 1
The dimension of TSVs and micropin-fins.

Dimensions	Diameter	Height	Pitch
Micropin-fin	150 μm	270 μm	225 μm
Through-silicon via	13 μm	300 μm	24 μm

to enable coolant delivery in and out of the dice. In such 3D ICs, the thickness of the silicon must be greater than the height of the micropin-fin heat sink. In general, micropin fins of a relatively large height are required in order to maintain an acceptable chip junction temperature under large power dissipation since the surface area of a heat sink increases as the heat sink height increases [10]. Moreover, it increases the hydraulic diameter of the heat sink and thus reduces the pressure drop. However, from an electrical perspective, this increased die thickness results in increased TSV dimensions (diameter and height) for a fixed aspect ratio TSV, as illustrated in Fig. 2. This in turn exacerbates the capacitance of the TSVs. The dielectric capacitance of TSVs can be expressed as [15]:

$$C_{ox} = \frac{2 \cdot \pi \cdot \varepsilon_{ox} \cdot h_{TSV}}{ln\left(\frac{r_{TSV} + t_{ox}}{r_{TSV}}\right)} \quad (1)$$

where ε_{ox} is the permittivity of silicon dioxide, t_{ox} is the thickness of silicon dioxide, r_{TSV} is the radius of a TSV, and h_{TSV} is the height of a TSV, respectively. Fig. 3 illustrates TSV capacitance and the maximum number of TSVs as a function of TSV aspect ratio for two die thicknesses (50 and 300 μm), assuming only 1% of the die area is allocated for TSVs. For the thinner (50 μm) die, which is in line with conventional 3D ICs, increasing the TSV aspect ratio does not significantly improve TSV capacitance. However, for thicker (300 μm) die, which is in line with the thickness needed for dice with embedded microfluidic cooling, the TSV aspect ratio plays a critical role in the electrical performance. If we increase the TSV aspect ratio from 5:1 to 20:1, the TSV capacitance decreases from 3.94 pF to 1 pF (an approximately 75% reduction). At the same time, assuming only 1% of the die area is allocated to TSVs, the maximum number of TSVs in the die increases from 353 to 5658. Thus, for silicon die with embedded microfluidic cooing, it is important to develop HAR TSVs to lower the capacitance and increase the number of interconnections between the tiers. This is missing in the literature and the focus of this paper. The following section describes our proposed TSV processes and their integration with the silicon micropin-fin heat sink.

3. The fabrication of high-aspect ratio TSVs in micropin-fin heat sink

The fabrication of TSVs within micropin-fins begins with a 300 μm thick double-side polished silicon wafer to enable the fabrication of 270 μm tall micropin-fins with a diameter of 150 μm. As will be discussed in this section, we demonstrate a 1 cm^2 die with 1936 micropin-fins, each containing 16 TSVs in a four by four array. The fabricated TSVs are 13 μm in diameter and 300 μm in height, which yields an aspect ratio of 23:1. Table 1 summarizes the dimensions of TSVs and micropin-fins. Fig. 4 illustrates the overall fabrication steps for HAR TSVs in micropin-fins. Fig. 4(a) illustrates a HAR silicon via etching step using two etch masks (either by an oxide mask or a photoresist mask), and Fig. 4(b) presents the fabrication processes following silicon via etching.

3.1. High-aspect ratio silicon via etch using two etch masks

The first step of the process is to etch narrow and tall silicon vias using the Bosch process, which alternates between passivation (C_4F_8) and etching (SF_6). This process step requires a precise procedure because the total area of vias to be etched is extremely small (e.g., 0.32%), which leads to a

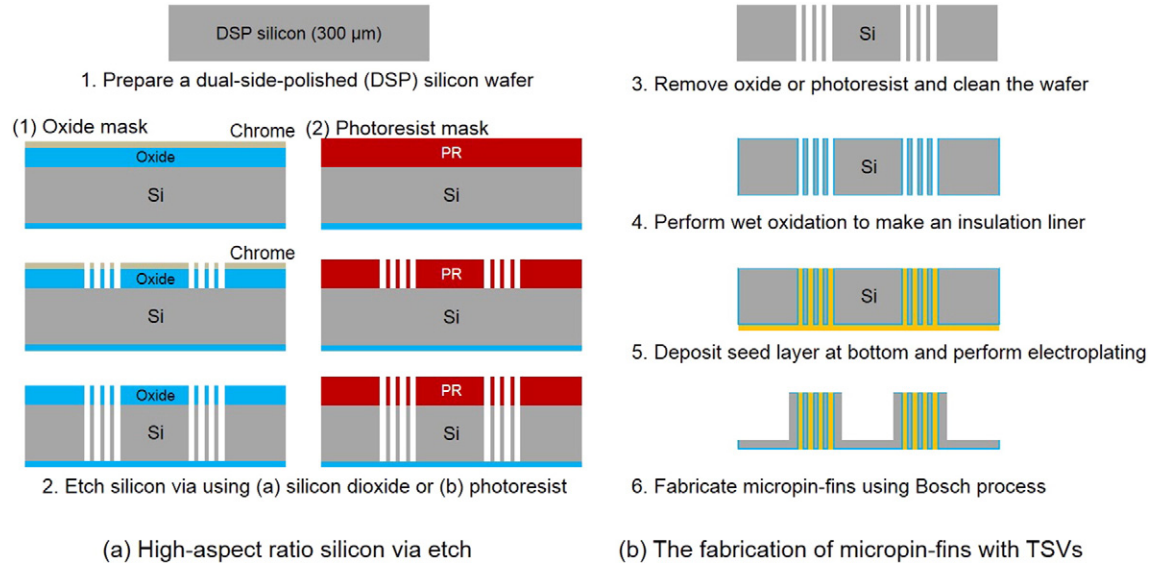

Fig. 4. An overview of the fabrication process of high-aspect ratio TSVs in a micropin-fin heat sink.

dramatic increase in the duration of etching, referred to as "RIE-lag effect" [16]. In addition, the time it takes to etch a silicon via does not proportionally increase as the via becomes deeper; rather, it becomes significantly prolonged for substantially deep vias. This effect occurs because the Bosch process is an aspect-ratio-dependent etch (ARDE), so the etch rate decreases dramatically for narrow and tall vias [17,18].

3.1.1. Hard mask (silicon dioxide)

To etch such deep vias with a small opening, we first optimized the Bosch process by increasing the coil power from 800 W to 2000 W. While this process dramatically decreases the silicon etch time, it requires the etch mask to be sufficiently robust to endure such high coil power. Thus, we use silicon dioxide as an etch mask, which has a higher selectivity than polymer-based masks [19]. At such a high coil power, the oxide mask exhibits high selectivity to silicon (>30:1), which indicates that we must deposit more than 10 μm of silicon oxide to etch a 300 μm thick silicon wafer. In order to pattern the silicon dioxide, we use a thin metal film as an etch mask instead of a polymer-based photoresist for two reasons: First, the metal film can be very thin (less than a micron) because of its high selectivity to silicon dioxide, while a photoresist mask is required to be as thick as the oxide (~10 μm). Second, the thin metal mask does not exhibit any sloped sidewalls as may occur in polymer-based etch masks.

To fabricate HAR silicon vias, we follow the process steps summarized in Fig. 4(a). First, we deposited a thick (~10 μm) silicon dioxide film using plasma-enhanced chemical vapor deposition (PECVD). Next, we sputter a thin (5000 Å) chrome film using physical vapor deposition (PVD) on the silicon dioxide, followed by etching chrome using the CR-7S chrome etchant. Fig. 5 shows an SEM image of the chrome-mask on the silicon dioxide. Using the patterned chrome as an etch mask, the silicon dioxide was etched by an anisotropic dry

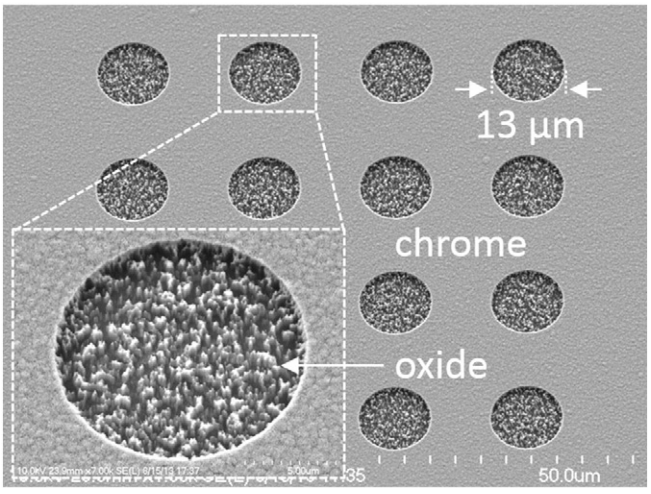

Fig. 5. Pattern of a chrome mask on silicon dioxide (oxide less than a micron is etched to distinguish the thin chrome layer from the oxide layer).

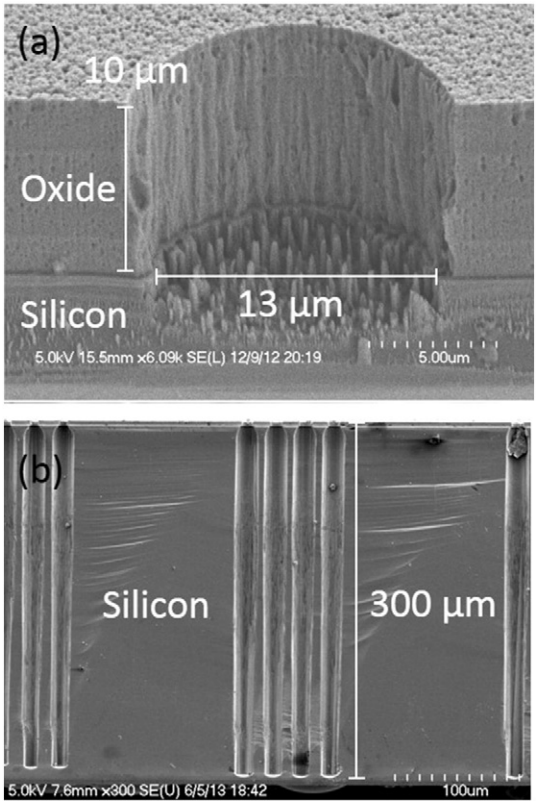

Fig. 6. (a) Cross-section of the etched oxide and (b) and the etched silicon using the oxide mask.

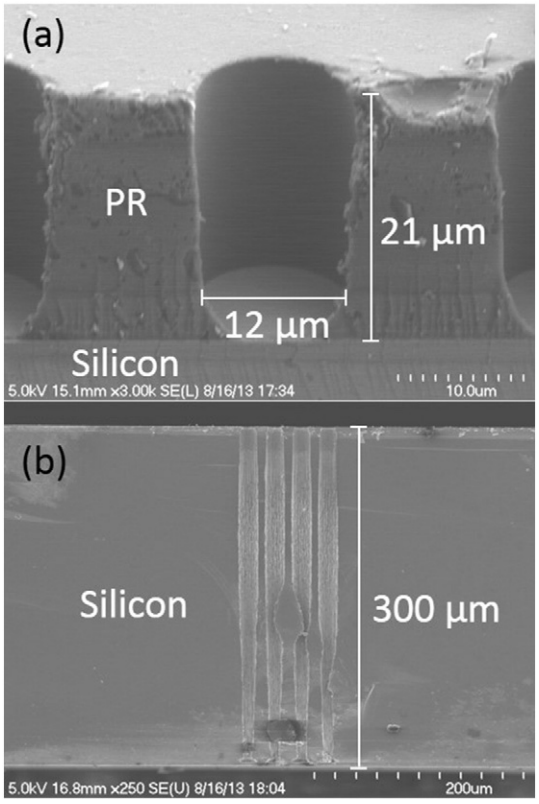

Fig. 7. (a) Cross-section of the photoresist mask and (b) etched silicon using the photoresist mask.

etch using the SPTS advanced oxide etch system. In this step, a coil power of 1800 W and a platen power of 180 W were set while the platen temperature was set to 60 °C, which helps increase the sidewall angle. Fig. 6 shows a cross-sectional view of the oxide mask after dry etching. Following the oxide etch, the silicon was etched using the SPTS Pegasus system with the optimization of etching parameters. During this step, as we continue to etch into the via, we slightly increase the etch duration from 2.5 to 3 s per cycle and increase the platen power from 75 to 85 W at 380 kHz to obtain a vertical sidewall profile. The coil power, which is one of the most critical parameters for etch rate, was increased to 2000 W. Etched silicon vias with a depth of 270 µm are shown in Fig. 6.

3.1.2. Soft mask (photoresist)

To simplify the fabrication process of the HAR silicon via etching, we also investigated silicon via fabrication using a chemically amplified photoresist, AZ-40XT (i-line positive photoresist) that can endure the total etch time. Fig. 7(a) exhibits a cross-sectional view of a 21 µm deep, 12 µm wide (aspect ratio of ~2:1) photoresist film. However, one limitation of using this photoresist is that it is not suitable for the high-power Bosch process (coil power of 2000 W). This is because the process consumes the photoresist so rapidly that the photoresist becomes depleted during the process. For this reason, we lowered the coil power to 800 W with a platen power of 17 W, which consumes

Table 2
Summary of the fabrication parameters used for silicon etching.

Coil power	2000 W (high)		800 W (low)
Mask	Oxide	Photoresist	Photoresist
Process	Complex	Simple	Simple
Etch rate	1.79 µm/min	N/A	0.92 µm/min
Selectivity	>30:1	Too low	~16:1

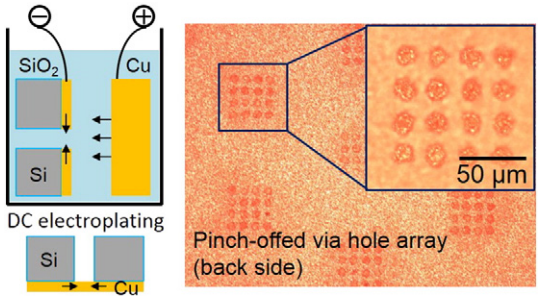

Fig. 8. Pinch-off via hole array by DC copper electroplating at the back side of the wafer.

less photoresist but also slows down the silicon etching considerably. Fig. 7(b) illustrates successful silicon via etching to a depth of 250 µm using a photoresist mask. Table 2 summarizes the results of both experiments.

3.2. The fabrication of a micropin-fin heat sink with embedded TSVs

After the removal of the remaining oxide on the silicon wafer, the second fabrication step begins with thermal oxidation to form an insulation liner for TSVs (~0.5 µm). Metal layers, titanium and copper, are deposited using an e-beam evaporator on the back side of the wafer for copper electroplating; titanium acts as an adhesion layer between the oxide and the copper. To pinch the etched holes, DC copper

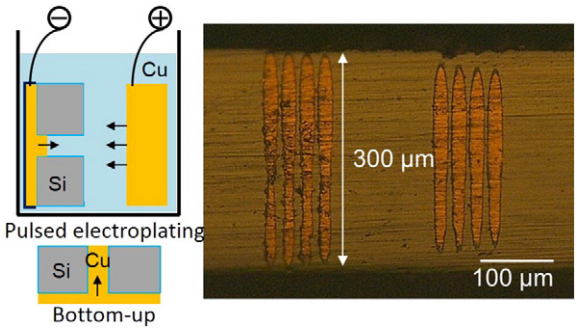

Fig. 9. Cross-sectional view of TSVs in a silicon wafer after 'bottom-up' copper electroplating, followed by CMP.

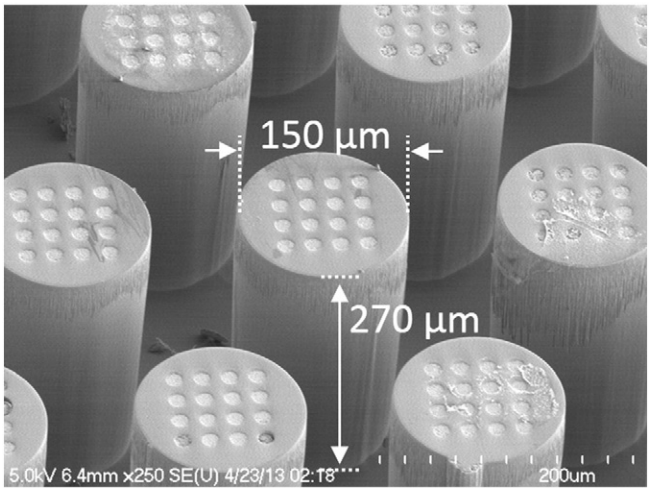

Fig. 10. SEM image showing an angled view of an array of micropin-fins with embedded TSVs.

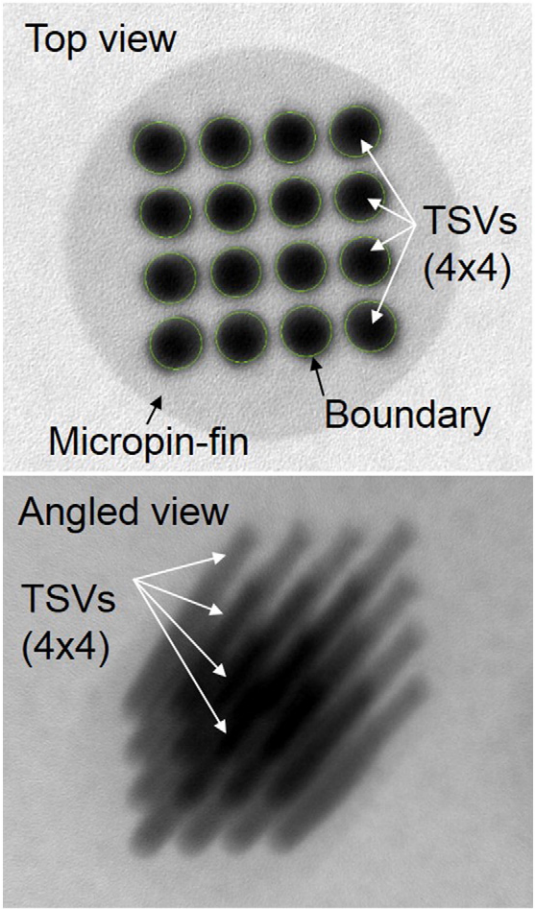

Fig .11. X-ray image of the TSVs in a micropin-fin from a top view and an angled view.

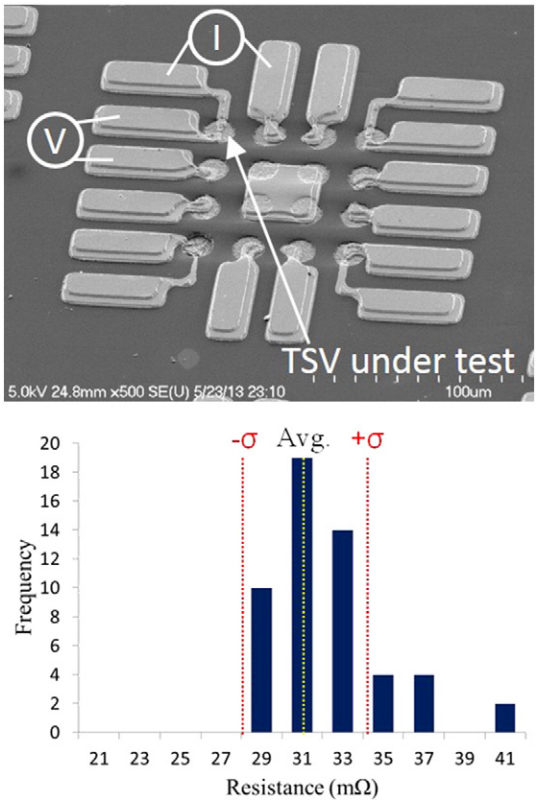

Fig. 12. TSV resistance measurements. SEM image of TSVs with fabricated pads and distribution of four point resistant measurements.

electroplating is performed with a current level of 10 mA on the back side of the wafer to form a seed layer, as shown in Fig. 8. Next, to fill the holes with copper, bottom-up copper electroplating is performed on the newly formed seed layer using Enthone DVF electroplating solution (Fig. 9). Bottom-up electroplating is useful to fill very high-aspect ratio vias [20]. In this process, pulsed-plating (60:40 on-and-off ratio) with a current level of 7 mA is performed to fill the vias without voids, which will be addressed at the next section. To remove over-electroplated and seed copper after electroplating, chemical mechanical polishing (CMP) was performed at the both sides of the wafer. Following polishing, the micropin-fin structure is fabricated using the Bosch process with a standard negative photoresist; this step is less sensitive to fabrication compared to the previous Bosch process, since the opening size of micropin-fin heat sink is quite large that it does not have the RIE-lag effect. The angled view of the fabricated TSVs in a 270 μm tall micropin-fin is shown in Fig. 10.

3.3. Verification of TSVs using four-point Kelvin technique and X-ray inspection

To verify void-free electroplating, we performed X-ray imaging. Fig. 11 illustrates top and angled view X-ray images of a single micropin-fin containing 16 TSVs (4 × 4 array). The X-ray image was taken from the top side of the sample to identify if voids were formed inside of TSVs during fabrication. On the left figure, the large dark gray circle is the micropin-fin, and the sixteen black circles are the TSVs in a 4 × 4 array. We first set the boundaries on the TSV regions (the solid borders surrounding TSVs in the figure), and we increased the voltage of the tool to 130 kV. If the TSVs contained voids, a white hole would appear in the TSV region. In addition, the resistance of the fabricated TSVs is measured using a Signatone probe station with the four-point Kelvin technique. To facilitate probing, we fabricated 50 μm × 20 μm metal (titanium/copper/gold) pads by PVD above the TSVs, as shown in Fig. 12. The final gold film was used to prevent the probing pads from being oxidized. The average measured resistance of a single TSV is 31.33 mΩ, with a standard deviation of 2.72 mΩ. Two methods (X-ray imaging and resistance measurements) verify the successful fabrication of void-free TSVs within the micropin-fin heat sink.

4. Conclusion

This paper demonstrates the integration of high-aspect ratio through-silicon vias (HAR TSVs) in a micropin-fin heat sink. We successfully fabricated 23:1 HAR TSVs within a micropin-fin heat sink using two different silicon etch masks. The benefits of hard mask (silicon dioxide) over soft mask (photoresist) are increased selectivity, which allows a thinner etch mask, and reduced silicon etch time due to higher platen and coil powers, though this comes at the expense of more demanding lithography process. Moreover, we verified void-free TSVs using X-ray inspection and four-point resistance measurements. These HAR TSVs promise to reduce the capacitance of the TSVs as well as to increase their density for fixed total footprint for the applications requiring microfluidic cooling.

Acknowledgments

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